Digital circuit blocks

E. J. van Barneveld

Digital techniques are being applied today in a wide variety of different fields. These include not only computers of various types and sizes, and data transmission equipment, but also industrial control systems. Since digital equipment is mainly made up of large numbers of comparatively few basic circuits, the construction of this equipment can be considerably simplified if the basic circuits are available in the form of "ready-made" units. This article describes a system of such "circuit blocks", marketed by Philips.

Digital equipment is generally made up of a limited number of types of basic circuit, such as gate circuits and bistable circuits, a large number of each type being used. Of course, it would be extremely uneconomical to design completely new basic circuits for every new piece of equipment, and, in fact, in the vast majority of cases, all that is needed is a combination of existing circuits. The next stage is that the basic circuits, instead of being built by the makers of the equipment themselves, are supplied complete by the electronic component manufacturer, i.e. by the supplier of the usual resistors, transistors, etc., and in a form in which they can easily be combined with one another to form a complete equipment. As the name implies these basic circuits are generally in the form of small blocks, provided with a number of pins by which they can conveniently be attached to a printed wiring board.

Although a circuit block is, as a rule, a little more expensive than the components of which it consists, a piece of equipment constructed from such circuits is less expensive than a similar one made up from conventional components. Several factors are concerned here. First of all, much less time and specialized knowledge is required for the design of a piece of equipment made up from circuit blocks. Secondly, the circuits take up less space; when the circuit blocks described in this article are used, twice as many circuits can be included on one printed wiring board as when separate components are used. Fewer boards, connectors, etc., are therefore required. Finally, this system makes the assembly and testing of the individual circuits much simpler.

Series of circuit blocks

Circuit blocks are usually supplied in a series of different types of matched circuit. The digital equipment from circuit blocks — mainly industrial measuring, regulating and control equipment — consists almost entirely of three main types of basic circuit, i.e. logic circuits, bistable circuits and trigger gates. In addition, there are various types of circuit such as input and output stages, delay circuits and clock pulse generators, which are used in only small quantities in each equipment. Although the number of different types is larger, these circuits do not usually amount to more than one-fifth of the total number of circuits. A series of circuit blocks should preferably contain all these types of circuit. If the series included only the most frequently occurring circuits — and this would at first sight seem an attractive proposition for the manufacturer — the makers of the equipment concerned would have to design all the other circuits themselves. In such a case, in spite of the use of circuit blocks, the design costs would be only very little lower than where *all* the circuits had to be designed by the equipment manufacturer.

A second reason why as complete as possible a range of circuit blocks is to be preferred is that the inputs and outputs of the circuits can then be matched, thus permitting the circuit blocks to be specified by a minimum of data and to be more readily combined.

This is the principle used in making up the series marketed by Philips. The oldest series, of which a few million units have already been made, is the "100 kHz series". The 10-series, with type numbers between 10 and 19, and the 20-series, with type numbers between 20 and 29, are of later design (see *figs. 1* and *2*). It is these latter two series that will be discussed here. They both contain the same basic circuits and are almost exactly alike in the construction of these circuits. *N-P-N* transistors are used in both ranges. The main difference between them is the semiconductor material used, which is germanium in the 10-series and silicon in the 20-series. Further, in the 20-series planar transistors are

Ir. E. J. van Barneveld is with the Philips Electronic Components and Materials Product Division, Eindhoven.

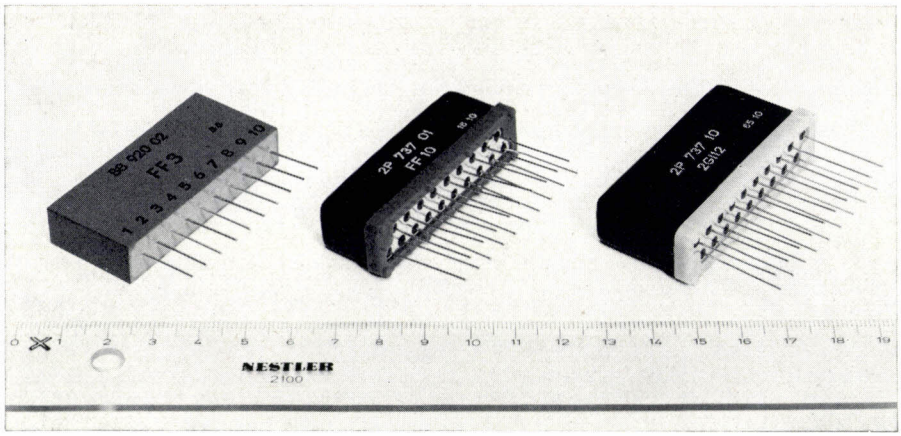

Fig. 1. The circuit blocks in the different series. On the left, a bistable circuit from the 100 kHz series, with beside it a bistable circuit from the 10-series and a block with two logic circuits from the 20-series. In the 10-series and 20-series a larger or smaller case is used according to the size of the circuit.

used, which have a higher cut-off frequency than the alloy transistors used in the 10-series. This permits a higher speed when using the 20-series blocks; some impression of the increased speed of operation may be gained from the fact that the maximum count rate of a bistable circuit is 1 MHz as against 30 kHz for the 10-series. The circuit blocks of the 20-series can also be used at higher ambient temperature; 85 °C is now permissible as against a maximum of 55 °C for the 10-series.

We shall now discuss various aspects of these series, paying particular attention to the measures taken to make the combination of the circuit blocks as simple as possible [1].

Combination of the circuit blocks

The basic circuits included in this series can occupy only two stationary states which correspond to the conducting and non-conducting states of one or more transistors in the circuit. These states are characterized by the voltage at one or more points in the circuit (for

[1] An article by Ir. C. Slofstra will shortly appear in this journal describing (for some applications) the design of a circuit using circuit blocks.

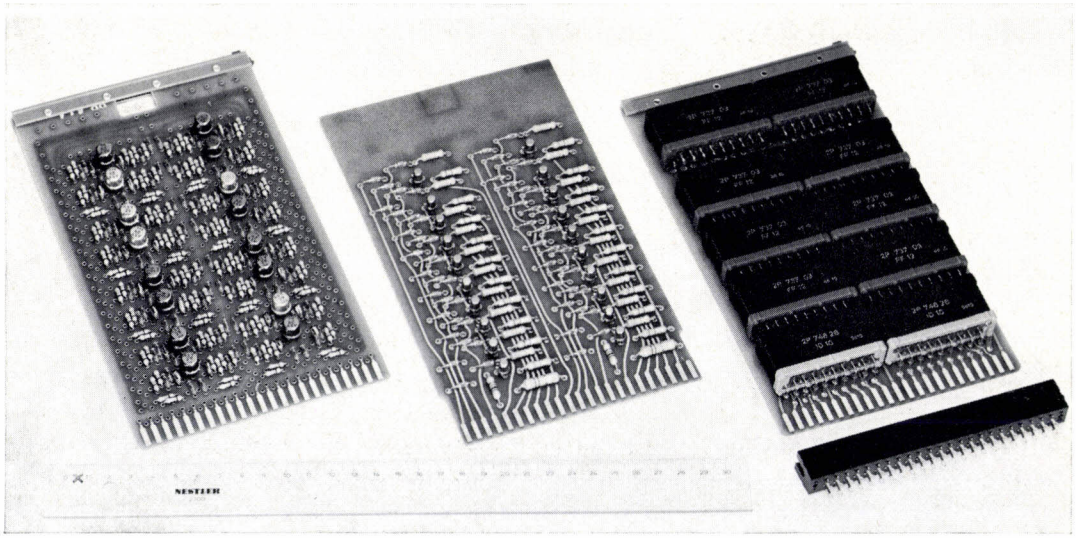

Fig. 2. On the right, some circuit blocks in the 20-series mounted on a printed wiring board. On the left, the same circuit made up from separate components, to illustrate the space-saving achieved with the blocks. With separate components, two printed circuit boards are required.

The boards are placed in a rack, where they fit into printed wiring connectors, one of which is visible in the foreground. The boards are connected together by means of wiring at the rear of the connectors.

instance the collector voltage of a transistor). In one state, indicated by H, this voltage is high (higher than V_H in *fig. 3*), and in the other, indicated by L, it is low (lower than V_L). Voltages between V_H and V_L cannot

Fig. 3. In digital circuits, in the steady state the output voltage is in one of the two ranges indicated by L and H. The signal temporarily enters the transition range only during the transition from L to H or vice versa.

occur continuously, but only during the transition from L to H or vice versa. In order to specify a circuit completely, V_L and V_H must therefore be given, together with the permitted output currents I_L and I_H for both states, and finally further details on the edges of the signal during the transition from L to H and vice versa. Six pieces of information are required for the output of each circuit and a further six corresponding ones for the input.

In combining logic circuits to form a larger unit, one must know the maximum number of inputs of other circuits which can be connected as a load at the output of one circuit. If a series contains only a few circuits, these numbers can be given in a table. *Table I* is the simplest possible table for an imaginary series of three circuits *A*, *B* and *C*. Where there is a mixed load, i.e. if it is desired to connect a number of different types of circuit to an output, this table does not give a definite answer. Therefore another table is often used, in which all allowed combinations are given. This next table is much larger (see *Table II*). Clearly, where the series contains a large number of circuits, the tables soon become unmanageably large, all the more so since some circuits have different kinds of inputs. In the present series, therefore, attempts have been made to limit the amount of information per input and per output so that a complex loading table is no longer required. It is intended rather that one should be able to calculate in a simple way from this data whether or not a certain load is permissible.

To limit the amount of information, the voltage levels V_L and V_H have first of all been made the same for all the circuit blocks. These need therefore only be given once and are of no further significance in combining the blocks. Furthermore, in this series the high-level current I_H is zero, apart from leakage currents, and only the slope of the negative-going edge of the signal in the transition from the high to the low level is of importance, so that there now remain only two pieces of information to be given for each input and output. We shall first show how these simplifications have been achieved.

The load in the steady state

If we consider only the steady state, we can distinguish between two kinds of load corresponding to the following kinds of circuit.

1) Current-delivering circuits. These deliver current to the driving stage if it is at the L level, i.e. if the output of this stage is at the low voltage. (We see that in this situation the "load" — i.e. the stage following the driving stage — *delivers* current!) They do not deliver a current to the driving stage if it is at the H level.

2) Current-drawing circuits. These draw current from the driving stage if this is at the high level, but not if it is at the low level.

	A	B	C
A	6	3	6
B	5	2	8
C	1	1	0

Table I. Loading table for a hypothetical series of three circuit blocks *A*, *B* and *C*. The figures in each column show the maximum number of circuit blocks of a certain type that may be connected to the output of a circuit block indicated at the left.

	A B C
A	6 + 0 + 6
	4 + 1 + 6
	2 + 2 + 6
	0 + 3 + 6
B	5 + 0 + 8
	3 + 1 + 8
	1 + 2 + 8
C	1 + 0 + 0
	0 + 1 + 0

Table II. An extension of Table I, in which mixed loading is taken into account. The maximum number of different inputs that can be simultaneously connected to one output are given.

Figs. 4 and *5* show examples of these circuits. The driving stage is represented by a transistor with a grounded emitter, as this form of output is used in all the circuit blocks in the series under discussion.

To obtain good loadability with current-drawing circuits, the collector resistance R_c must be low. This, however, means that, if the transistor is conducting, a large current passes through R_c, so that only a few current-delivering circuits can be connected. A higher R_c is better for current-delivering circuits but not for current-drawing circuits. The loadability is distributed over both types by fixing the value of R_c. This compromise will, of course, not be optimum for most

cases. Moreover, this distribution leads to complex loading tables like those mentioned above.

To avoid these difficulties, only current-delivering circuits are used in the circuit blocks described here; this means that the current at high level is always zero, as stated above. At first sight it would appear to be impossible to make up certain circuits with these circuit blocks. This is not so, however, since a current-drawing circuit can easily be converted into a current-delivering circuit by the addition of two resistors and a blocking diode (see *fig. 6*). In fig. 5 the current for the load is supplied via the collector resistance of the driving stage and in fig. 6 this current is supplied via the resistor R_1, while diode D prevents current from being drawn from the driving stage. The new circuit thus provided can only *deliver* current to the driving stage and only if the latter is at the low level.

This simplification makes it sufficient to specify only one current per input and per output in the steady state, and this is the current which flows in the L state. This makes the loading table much simpler. The maximum current which may flow through it is given for each output, for each input the current it delivers is given. For the purposes of checking whether a given load is permissible, all that need be done is to add the currents of all the inputs connected to a certain output and see whether this exceeds the permissible output current. As the input currents of most of the circuit blocks are the same, all that usually has to be done is to count the number of inputs. This additive system of loading represents a great simplification, especially with mixed loading.

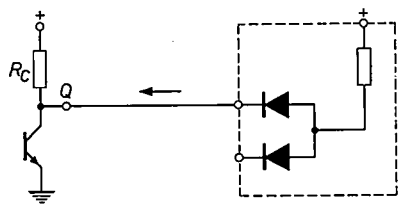

Fig. 4. Example of a current-delivering circuit (in the "box"). If the transistor in the driving stage is conducting and the voltage at the output Q is therefore at the low level, current flows to the left through the output. If the transistor is cut off (with the output at the H level), the current is zero.

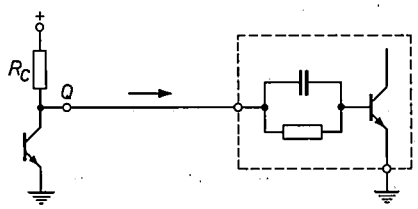

Fig. 5. Example of a current-drawing circuit (in the "box"). If the transistor in the driving stage is conducting (output Q at L level), no current flows through the output. If the transistor is blocked, current flows to the right.

Now that current-drawing circuits are not being taken into acount, the value of the collector resistor R_C can be made so high that the maximum number of current-delivering circuits may be connected to an output.

There are two further advantages in the use of the blocking diode. The first is that there is an anti-noise threshold voltage across this diode. To see how this operates, let us consider the state where the driving transistor is non-conducting. The output Q is then at

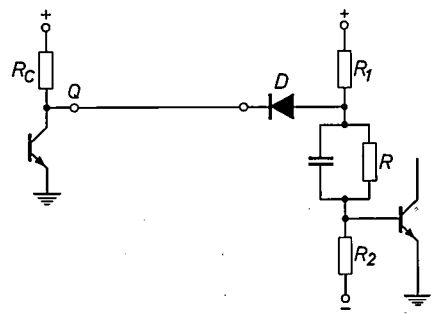

Fig. 6. The current-drawing circuit in fig. 5 can be converted into a current-delivering circuit by the addition of a blocking diode D and two resistors R_1 and R_2. This also produces a threshold against interference since the left-hand side of D is at a higher voltage than the right-hand side.

the supply voltage and the driven transistor is conducting. If a negative noise pulse now occurs in the connection between the stages, it can block the driven transistor in the situation illustrated in fig. 5. In the situation given in fig. 6, the supply voltage is applied to the left-hand side of the diode D. The voltage on the right-hand side of the diode is lower, however, because of the voltage division due to resistors R_1 and R. There is, therefore, a voltage in the reverse direction across the diode. Noise pulses can affect the second stage now only if they overcome the diode reverse bias. If however the driving transistor is conducting, it forms a low impedance to earth; the interfering pulses picked up on the connections are then small enough not to affect the next stage.

A second additional advantage of the use of a blocking diode is that by connecting a few more diodes in parallel a logic circuit (AND or OR function) can very easily be obtained. This will be discussed further later on.

To summarize, the most important advantages of limiting the units to current-delivering circuits are:

1) great loadability (fan-out);
2) only one piece of information is needed for each input and output for the stationary state, and hence the loading table is simple;
3) the loads are additive, so that it is a simple matter to check mixed loads;
4) the circuits are less sensitive to interference;
5) it is very easy to add a logic function.

Transient charges

The loading table must also provide information on the signal edges. Here we are faced with the same problem as with the steady state, i.e. that the table threatens to become complex, particularly with mixed loads. At the inputs of some circuits, particularly at the inputs of the trigger gates, the transition from the high to the low voltage must take place within a very short time. When different circuit blocks are combined, therefore, the question once more arises of whether the driving stage can provide a sufficiently steep edge, and the loading table should provide the answer. (In the transition from the low to the high voltage, the transition time does not critically affect the operation of the circuits.)

In assessing the edge steepness of the transition from the high to the low voltage, use is made of the concept of "transient charge" defined as follows. At the high voltage, no current flows through the output of the driving stage (see fig. 6 again), while current does flow at the low voltage. The load then supplies current to the driving stage. During the signal transition, the current through the output thus increases from zero to a certain final value. This means that, during this time, a given charge flows through the output of the driving stage. For each output this "transient" charge has a certain maximum which can be calculated from the transistor data.

The transient charge is absorbed by the load. If this is capacitive, it is clear that, during the transient, a *clearly-defined* charge will be required which must be supplied by the driving stage. The magnitude of this charge is $C\Delta V$, where ΔV is the difference between the voltages across the capacitor before and after the transient. For a resistive load also the charge flowing during the transition from high to low voltage can be calculated from the final value of the current and the time taken by the voltage transition. Both kinds of load can therefore be characterized by one quantity, i.e. the charge displaced. The loads are thus also additive under non-steady-state conditions.

The procedure for checking a given combination of circuits is now the same as for the steady state. The transient charge is given for each output and input, the charges belonging to the inputs connected to one output are added together and a check is made to see whether the total charge is less than the output can supply. If so, the transition time will be shorter than needed for the trigger gate, and correct operation will be ensured.

There is one difference in checking the current load. The currents must always be checked, whereas the transient charges need to be checked only if inputs of trigger gates are connected to an output. If this is not the case no special requirements are set for the transient.

The complete loading table thus consists only of figures giving one current and one transient charge for each input and output in the system. We give this table here for the circuit blocks of the 10-series; see *Table III*. (The symbols G, T and S indicate the different types of input; these will be dealt with later in this article. The outputs are indicated by Q, or by Q_1 and Q_2 if a circuit block has two.) Thirty-eight pieces of information are required for the complete specification of nine basic circuits. The simplest loading table of the Table I type would require for this 88 pieces of information, since there are 11 different inputs and 8 outputs, and this would still give no definite indication on mixed loads, such as is given by Table III.

Table III. The loading table for the 10-series.

Type	Input terminal	Direct current mA	Transient charge nC
FF11, FF12	G	1.1	1.2
2.TG13, 2.TG14, 4.TG15	T	1.1	3.4
FF10, FF11, FF12	S	1.95	2.8
2.GI10, 2.GI11, 2.GI12	G	1.1	2.1
GA11	G	1.1	1.2
OS11	G	1.1	1.2
	T	1.1	2.3
TU10, PD11	G	1.1	1.2
	T	1.1	3.2
RD10	G	4.7	3.4
PA10	G	5.3	5.2

Type	Output terminal	Direct current mA	Transient charge nC
FF10, FF11, FF12	Q_1, Q_2	8.2	27
2.GI10, 2.GI11, 2.GI12	Q	8.2	9
GA11	Q	62	75
OS11	Q_1	8.6	24
	Q_2	12.8	29
TU10	Q	32	27
PD11	Q	100	185
PS10	Q	10	39

We shall now take a look at the various types of basic circuit included in the series. We shall see here the consequences of the measures discussed, in particular of the limitation to current-delivering circuits.

Logic circuits

It often happens in digital circuits that the voltage at a certain point must be high or low depending on whether there are certain combinations of voltages at a number of other points. These voltages are then applied to the inputs of a "logic circuit", i.e. a circuit designed

in such a way that the desired voltage appears at its output if the input voltages satisfy the appropriate conditions.

The name "logic circuits" is derived from the fact that the relationship between the input and output voltages of these circuits can be described by logic functions from Boolean algebra — the algebra which is used for calculations with elements that can operate in only two stationary states. A letter is allocated to each element in exactly the same way as in ordinary algebra, and the two states are indicated by "0" and "1", e.g. A = "1" or A = "0". The interdependence of different elements can also be expressed here by a function, e.g. $Z = AB + CD$. The significance of a function is however slightly different from its usual meaning. In this algebra all the functions, which are also called operations, can be broken down into three basic functions:

In breaking down an involved logic function, we can use the rules of De Morgan, which are given here without proof:

$$\overline{A} + \overline{B} + \overline{C} + \ldots = \overline{A.B.C.\ \ldots}$$

and

$$\overline{A + B + C + \ldots} = \overline{A}.\overline{B}.\overline{C}.\ \ldots$$

The commutative and distributive rules can also be used, just as in algebraic processes.

As logic functions can be broken down into the three basic functions, so can logic circuits be composed of three basic circuits, namely the AND, OR and NOT circuits. These basic circuits can be electrically constituted in a number of ways. One of the most usual is to use diodes and transistors (Diode-Transistor-Logic, or DTL). *Figs. 7a, b* and *c* show the three circuits. For purposes of simplicity, the AND and OR circuits are shown with only two inputs, although there can be more.

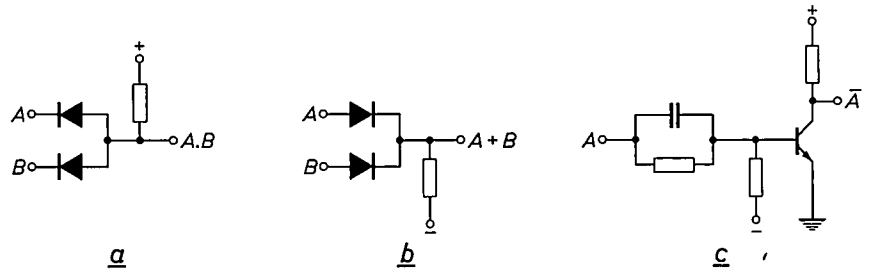

Fig. 7. *a*) The AND circuit. The output here is at a high voltage (state "1") only if the voltages at *A and B* are high. *b*) The OR circuit. Here, the output is at a high voltage if either *A or B* (or both) are at a high voltage. *c*) A transistor connected up as an inverting amplifier operates as a NOT circuit. If the input voltage is high, the transistor conducts and the output voltage is low.

"AND", "OR" and "NOT". In the AND function, designated by $Z = A.B.C. \ldots$, Z is in state "1" if all the elements, i.e. *A and B and C etc.*, are in state "1". For the OR function ($Z = A + B + C + \ldots$), Z is in state "1" if one or more of the components, i.e. *A or B or C*, or *A and B*, etc., are in state "1". The NOT function $Z = \overline{A}$ gives an inversion, i.e. Z = "1" if A = "0" and Z = "0" if A = "1". The function $Z = A.B + C.D$ given above as an example therefore has the following significance: Z = "1" if *A and B, or C and D*, or *A and B and C and D* are "1". The AND and OR functions can be given in the form of a "truth table". *Table IV* gives this table for two components A and B.

Logic functions are written in such a way as to provide as great a degree of correspondence as possible with ordinary arithmetical processes: if A = "1" and B = "0", then $A.B$ = "0" and $A + B$ = "1", just like ordinary multiplication and addition. The only exception is formed by the case A = "1", B = "1"; now $A + B$ is not 2, as one would expect, but "1".

Table IV. Truth table for the AND function $A.B$ and the OR function $A + B$.

A	B	$A.B$	$A+B$
1	1	1	1
1	0	0	1
0	1	0	1
0	0	0	0

Because the AND and OR circuits may also be regarded as gate circuits, i.e. a voltage at one input is allowed to pass through to the output only if there is a certain voltage at the other input, the terms AND gate and OR gate have also come to be used.

"Positive logic" has been chosen for the examples in fig. 7; that is to say, state "1" is allocated to the high voltage level. This "logic convention" could equally

well have been reversed, i.e. state "1" could correspond to the low level. In such a case, the terminology as applied to the circuits would also be reversed. Fig. 7*a* is then an OR circuit, since the output is at the low level as soon as one of the inputs is negative, and fig. 7*b* is, then, an AND circuit. Table IV also shows that the AND and OR function can be interchanged in this way.

Regardless of the logic convention chosen, be it positive or negative logic, one of the two circuits, AND or OR, is always a current-delivering circuit (fig. 7*a*) and the other a current-drawing circuit (fig. 7*b*). This situation is not permissible in the logic circuits used in the series discussed here. The solution found to this problem amounts, in fact, to the use of mixed logic, i.e. positive or negative, as required, so that both the AND and the OR function can be obtained with one basic circuit. The current-delivering circuit is used here as the basic circuit (an AND circuit with positive logic) followed by an inverting amplifier (*fig. 8a*). This circuit is referred to as a NAND circuit, the term being a contraction of the words NOT and AND, just like NOR as the term for the combination of a NOT and an OR circuit. With this one basic circuit, all possible logic circuits can be constructed.

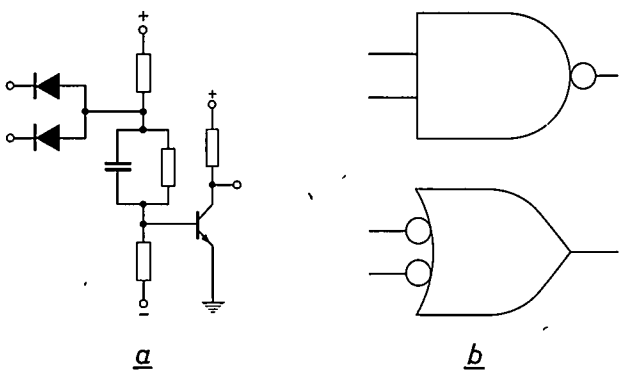

Fig. 8. *a*) The NAND circuit. *b*) The symbols indicating the NAND circuit as an AND function (upper symbol) and an OR function (lower symbol). A circle at an input or output indicates that the voltage at that point is low if the condition is fulfilled.

The method of working with this logic unit can most simply be described with the aid of a truth table using the voltage levels H and L at the inputs and at the output [2], instead of the states "0" and "1", which change depending on whether positive or negative logic is used. *Table V* gives this truth table for the NAND circuit in fig. 8*a*. It will be seen from the table that the output voltage is low only if both input voltages are high. The NAND circuit therefore operates as an AND circuit at the *high* level — i.e. if voltages are applied to it that are high in the desired state — the output voltage being low. This is indicated by the upper symbol in fig. 8*b*, where the circle at the output indicates that this is at the low level if the AND condition is satisfied. The table also shows that the output voltage is high if either or both of the input voltages are low. The NAND circuit therefore operates as an OR circuit at the *low* level — i.e. if voltages are applied which are low in the desired state —, the output voltage being high. This is indicated by the lower symbol in fig. 8*b*, the circles at the inputs showing that this function operates at the low level, while the absence of a circle at the output shows that the output voltage is high if the input condition is satisfied.

Table V. The truth table for the NAND circuit in fig. 8*a*.

inputs		output
H	H	L
H	L	H
L	H	H
L	L	H

The NAND circuit can also be separately used as a NOT circuit; the signal to be inverted must then be applied to one of the inputs. This is because an unconnected input behaves as if the high voltage is applied to it (in both situations the diode does not conduct). If we now apply a signal at one input and do not connect the other, this signal appears at the inverting circuit of the NAND (the AND gate is now always open) and the inverted signal appears at the output of the NAND.

The NAND circuit therefore enables all the basic logic circuits to be obtained, provided that the input signals can be supplied with the correct polarity. In some situations it may first be necessary to invert the input signals, but in practice this is seldom required. Signals of both polarities are usually available, especially if they originate from bistable devices.

An example of the construction of more complicated logic circuits is given by the various possible circuits for obtaining the function $\overline{A.B + C.D}$. *Fig. 9* shows this function obtained in the conventional way with two AND and one OR circuits and an inverting amplifier.

[2] This method of approach and the symbols that we shall use here have been taken from the American military standard MIL-STD-806B, described in: F. Flanagan, Standardization of logic diagrams, Computer Design 3, No. 7, 12-19, 1964; see also American Standard Graphical Symbols for Logic Diagrams, Y 32.14, American Standards Association.

[3] R. E. Burke and J. G. van Bosse, NAND-AND circuits, IEEE Trans. on electronic computers **EC-14**, 63-65, 1965.

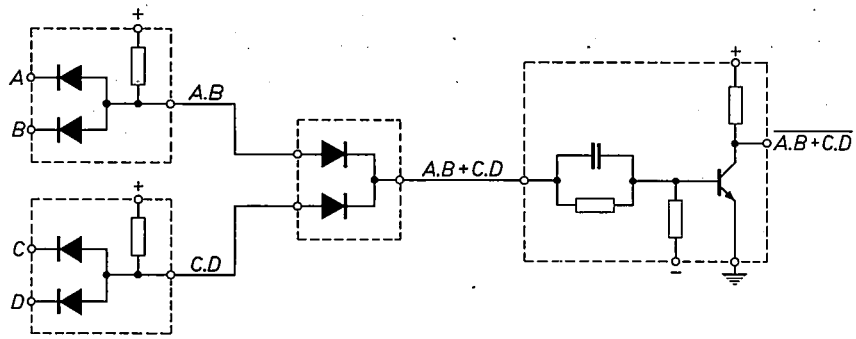

Fig. 9. The logic function $\overline{A.B + C.D}$ produced with AND and OR circuits and an inverting amplifier.

Fig. 10 illustrates the circuit made up from three NANDs. Here, however, the polarity of the output signal is incorrect, so that an inverting amplifier would be required. It is possible however to make two NANDs suffice by connecting the collectors of the output transistors in parallel (*figs. 11a* and *b*)[3]. The two transistors now form an OR circuit. The common output has a low voltage if either of the transistors conducts. The disadvantage of this circuit is that the functions $A.B$ and $C.D$ are no longer available separately. We therefore see that the function $\overline{A.B + C.D}$, which requires four units with the conventional technique, can be made up from two NANDs.

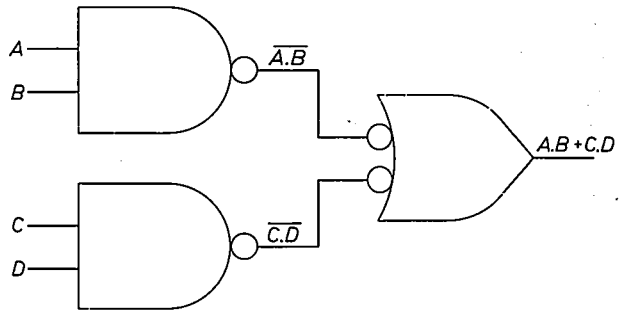

Fig. 10. The logic function $A.B + C.D$ obtained with three NAND circuits. To make $\overline{A.B + C.D}$, an inverting amplifier must be added.

A great advantage of the NAND system is that the voltage levels H and L are always the same. This is not so in fig. 9. If the input voltages here are 10 V, the voltages at the inputs of the second stage are 4 V, for example. As long as there is no amplifier in between, the difference between the high and low voltage will decrease with every stage. In the NAND system, however, there is further amplification in each stage, so that the same voltages occur throughout the equipment. This means that a voltage may be taken out anywhere in a system and used directly for another circuit; the tracing of faults in such a system is also much simpler.

One objection to the use of this method could be raised: this is that more transistors are necessary than in the normal system. Every stage, in fact, now contains an inverting amplifier, while otherwise ampli-

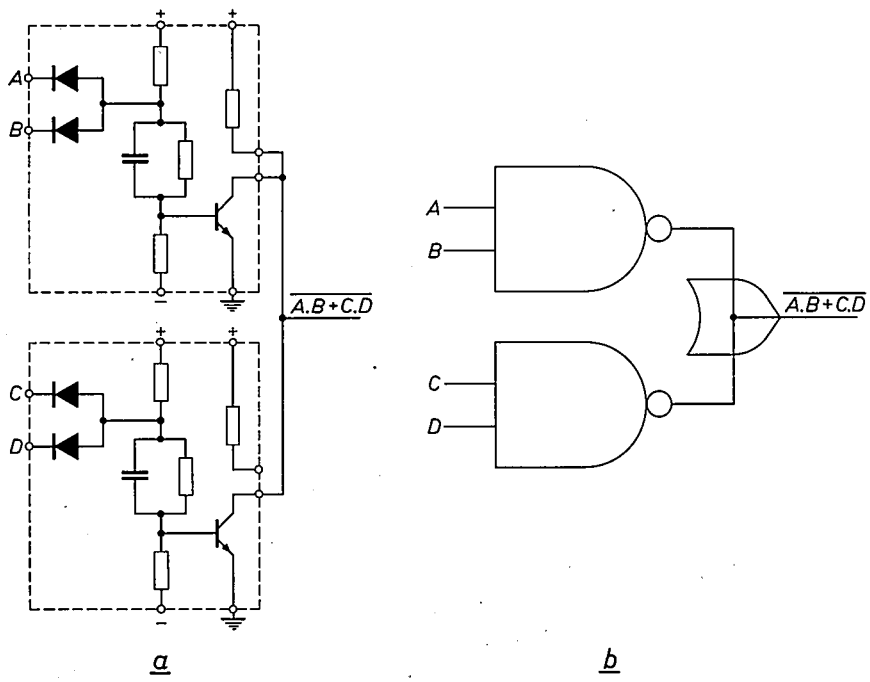

Fig. 11. *a*) The logic function $\overline{A.B + C.D}$ can be directly obtained with two NAND circuits by connecting the collectors of the output transistors in parallel. No separate circuit is then required for the OR function. Here the collector resistor of only *one* NAND-circuit is connected; this is done to get a lower current consumption and thus a higher loadability. *b*) The circuit in symbols.

fication often takes place only after every two stages (see fig. 9). The NAND technique could therefore be more expensive in use. This point has been investigated by comparing conventional and NAND designs in a few practical cases, including a digital computer [4]. The expected difference in cost was indeed found but it was too small to offset the considerable advantages of the NAND system.

We can recapitulate the most significant advantages of the use of NAND circuits as follows.

1) The advantages of the restriction to current-delivering circuits are also of course applicable here, the high degree of loadability being of particular importance.

2) All voltages in the system are standard voltages. Thus, every output voltage can be used at various points.

3) Fewer units are generally needed to make up a given circuit than when other basic circuits are chosen. This means that fewer circuit blocks, printed wiring boards, connectors, etc., are required.

4) Because of the restriction to one kind of circuit, not only are fewer units needed to make a piece of equipment but also fewer different types are required. This simplifies manufacture and servicing and reduces the number of spares required.

The last two points contribute most to the economic attraction of the NAND circuit.

The bistable circuit and the trigger gate

We should now like to consider further the bistable circuit and the trigger gates used in this series of circuit blocks. The bistable circuits (flip-flops) are of the "decoupled" type (see *fig. 12*). They consist in fact of two NAND circuits cross-coupled via diodes D_1 and D_2. These diodes have two functions. First, there is a threshold voltage across each diode to counteract noise and secondly they facilitate the switch-over of the bistable circuit.

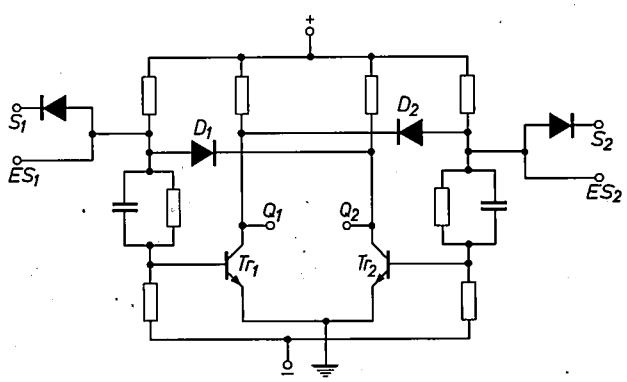

Fig. 12. A "decoupled" bistable circuit of the type included in the range (unit FF10 in the 10-series). The circuit consists of two cross-coupled NAND circuits. The circuit can be made to switch over by taking the S input of the conducting transistor to the low level.

The threshold voltage is the same as that discussed in the general treatment of the current-delivering circuit (page 47). Diodes D_1 and D_2 are, in fact, blocking diodes in current-delivering circuits. Here, the thresholds prevent a negative pulse at the output of the non-conducting transistor from arriving at the input of the conducting transistor, which could cause the bistable circuit to change its state. The name of this type of circuit comes from this "decoupling" effect provided by the diodes. The insensitivity to noise is very important in a bistable circuit. If it changes state as a result of a noise pulse, it will remain in this incorrect state even after the interference has ceased.

The bistable circuit can very easily be made to change state if the input S (S for "set") on the side of the conducting transistor, e.g. S_1 for Tr_1, is taken to the low level. The base voltage of this transistor then becomes negative, the collector current becomes zero, and the output voltage Q_1 increases so that Tr_2 now begins to conduct and because of its low output voltage maintains Tr_1 in the cut-off state. This has thus brought the bistable circuit into its other stable state. If no decoupling diodes are used, the difficulty arises that, on changing state, not only point S but also the inputs of all circuits connected to Q_2 must be taken to earth potential. This is quite permissible for one bistable circuit, but if several are to be made to change over simultaneously — and this is often the case — an undesirably high current may be necessary and the speed of the change-over will be adversely affected. The S inputs show considerable similarity to the inputs of a NAND circuit. Supplementary diodes can be connected to the ES inputs (E for expander), enabling the number of inputs of a bistable circuit to be increased.

The bistable circuit is often used in combination with trigger gates, which ensure that a pulse can only cause the bistable circuit to change state if a certain condition is met.

Realization of the trigger gate

In its simplest form, the trigger gate consists of a capacitor, a resistor and a diode. Such a circuit is connected to the base of each of the transistors in a bistable circuit (*fig. 13*). Let us take Tr_1 to be in the conducting state and consider the trigger gate connected to this transistor. The base voltage of Tr_1 is close to earth potential. Let us now assume that point G_1, the condition input, is also roughly at earth potential and that T_1, the trigger input, is at the high level. The left-hand side of capacitor C_1 is now at a positive voltage and the right-hand side is at earth potential, and diode D_3 is reverse-biased. If now the voltage at T_1 falls (H $\rightarrow$ L), the right-hand side of C_1 goes negative for a moment, the diode starts to conduct and thus takes

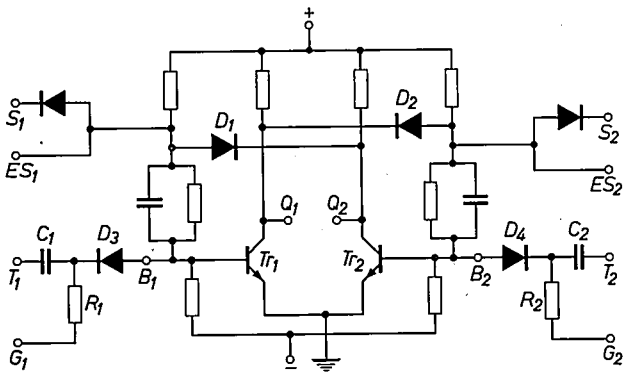

Fig. 13. The bistable circuit of fig. 12 with two simple trigger gates. G_1 and G_2 are the condition inputs, T_1 and T_2 the trigger inputs and B_1 and B_2 the base inputs of the bistable circuit.

up the base current of the transistor. There is then no transistor current for a short time and, if C_1 and R_1 are of the correct values, this period is sufficient to cause the bistable circuit to change state. If however we start from the situation where G_1 is at the high voltage, both sides of C_1 are at this high voltage. If the voltage at T_1 falls there will indeed be a fall in voltage at the right-hand side of the capacitor, but this does not go negative. The diode therefore remains reverse-biased and the bistable circuit does not change over.

Both the trigger inputs T_1 and T_2 of such a bistable circuit can be permanently connected to a clock pulse generator delivering pulses at a certain frequency to the inputs. The bistable circuit can then be set to a desired state by making the voltages high or low at the condition inputs G_1 and G_2. The condition may also be derived directly from the bistable circuit, e.g. by connecting each condition input to the output of the transistor to which the trigger gate is connected (i.e. G_1 to Q_1 and G_2 to Q_2). If the two trigger inputs are now connected together, and if a series of pulses is applied to them, the bistable circuit is triggered by every pulse. The circuit now operates as a binary scaler. This is an important and often-used application.

Irrespective of the voltages at the inputs G and T, the bistable circuit can be set in a certain position by bringing one of the S inputs to earth potential. This is mainly used for setting the circuit in the zero position.

The simple trigger gate has several drawbacks which make it necessary to design a more complicated circuit for the units described here [5]. In the first place, a voltage change at one of the inputs T or G produces a current pulse at the other input, and this current can flow in either direction. The effects of this on the circuit connected to this input can be undesirable, and are hard to prevent. Moreover, this bi-directional current does not suit our desire for a system with only one kind of load.

A second objection is that the response time of the circuit is very largely governed by previous conditions. If, for example, T has been at a low voltage and G at a high voltage for some time, capacitor C is charged. If now both voltages change, a long time will elapse before the charge state of the capacitor changes and a steady state holds once more. If however only one of the voltages changes, the response time is shorter. It is also very difficult to calculate the response times because of the effects of the capacitance of the wiring and the collector resistances of driving stages.

These objections can be partly overcome by requiring that, if the voltage at the condition input is to change, it must do so immediately upon the arrival of a trigger pulse at input T. This is known as synchronous operation. The likelihood of the following trigger pulse occurring before the circuit has returned to the steady state is then as small as possible. Such requirements however cannot always be made.

These drawbacks do not occur with the trigger gate circuit shown in *fig. 14*, which is used in our series.

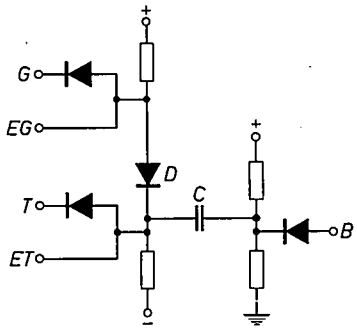

Fig. 14. The trigger gate circuit used in the circuit blocks. G is the condition input, T the trigger input, and B is connected to the base input of a bistable circuit.

The central point in this circuit is, once again, a capacitor C. The right-hand side of this capacitor is taken by the voltage divider to a voltage close to earth potential. If both G and T are at the high level, the left-hand side of the capacitor is at a high voltage. If the voltage at point T now falls sharply from high to low, the voltage at the right-hand side of C falls for a short time below earth potential, thus causing the bistable circuit to change over in the same way as in the simple circuit.

The capacitor is charged only when both G and T are at the high level. If G is at earth potential and T is at the high level, diode D is blocked so that the left-hand side of C is taken to approximately earth potential by the negative voltage. If the voltage at T is now also taken to earth potential, nothing happens, since the diode at T does not become conducting. The trigger gate is thus opened if G is at the high level and closed if G is at the low level.

[4] For this last case the research was undertaken by Dr. N. C. de Troye of Philips Research Laboratories, Eindhoven.

[5] See N. O. Sokal, Trouble-spots in circuits, Electronic Design **12**, No. 23, p. 32, 1964.

In this circuit, a voltage change at one of the inputs T or G is clearly not noticeable at the other input. Moreover, the response time at a change in voltage at point G now depends solely on the value of the capacitance and the resistances of the circuit. These values may be so selected that the response times on opening and closing are equal. There need therefore be only one response time to be taken into account, and this can be calculated precisely and is independent of previous conditions.

Yet another facility is offered by the circuit of the trigger gate of fig. 14. It is possible to connect diodes at input EG in parallel with the diode at G, thus, in a very simple way, providing an AND circuit. The trigger gate is now opened only if there is a high voltage on *all* these diodes. An OR function can also be produced by connecting a few trigger gates in parallel. Such facilities can be very important in practice. The number of trigger inputs of a trigger gate can be increased in the same way as described for the G inputs and for the S inputs of a bistable circuit, i.e. by connection of additional diodes at point ET. The pulse gates are included in the series as independent circuit blocks, but bistable circuits are also available which already have two trigger gates (*fig. 15*).

An AND circuit with a non-inverting amplifier (GA, gate amplifier). The loadability of this circuit is much greater than that of the GI circuit.

Two circuits providing a time-delay. Both comprise a trigger gate and a monostable circuit. The type OS (one-shot multivibrator) gives a delay time of 4 μs to 30 ms, the type TU (timer unit) gives longer times, up to 60 s. Both circuits attain their longest delay time by the addition of an external capacitor.

A clock pulse generator (PD, pulse driver), consisting of a trigger gate followed by a monostable circuit.

A Schmitt trigger by means of which pulses can be properly shaped in slope and height (PS, pulse shaper).

Two different output amplifiers, one for low powers (RD, relay driver), and one for higher powers (PA, power amplifier).

A circuit that decodes the position of a decade of a binary counter and controls a decimal indicator tube (ID, indicator tube driver). As this circuit is only intended to be controlled by a counting decade, it is not given in Table III. Two of these circuits together with two decades each of four bistable circuits are shown on the printed wiring board in fig. 2.

The 20-series includes the same types, but there the

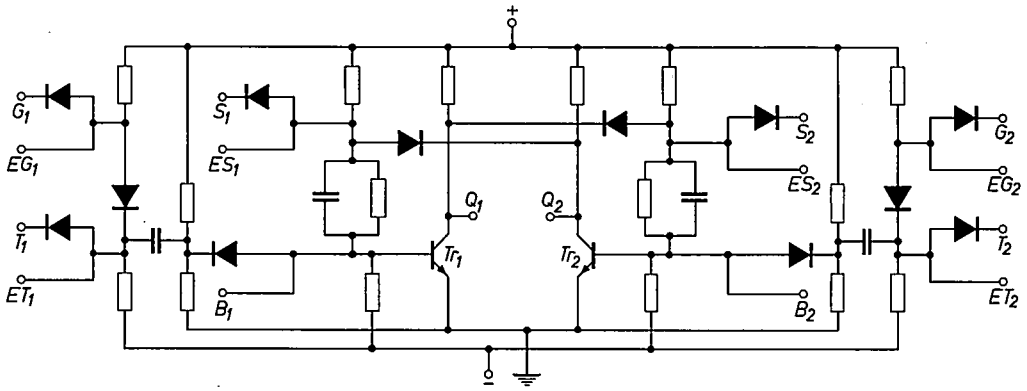

Fig. 15. A bistable circuit with trigger gates mounted in one circuit block (type FF12).

The other circuit blocks in the series

Table III gives a survey of the various types of circuit blocks in the 10-series. The inputs are classified in the manner used above: trigger inputs of trigger gates, T; condition inputs and inputs of NAND circuits, G; set inputs, S. The outputs of the circuits are called Q, or Q_1 and Q_2 if there are two.

The 10-series includes three circuit blocks with a bistable circuit, given the type indication FF (from "flip-flop"), one without and two with trigger gates. There are also three circuit blocks with two or four trigger gates (TG) and three with two NAND circuits (GI, gate inverters). We shall now briefly list the other circuit blocks in the 10-series.

GA is replaced by a GI with a greater loadability. There are also circuit blocks for controlling and reading out from stores and for transmitting and receiving information via a cable.

Power supply equipment to suit the series is available, as are also a number of standard printed wiring boards with racks into which they can be fitted.

Construction of the circuit blocks

The internal arrangement of the circuit blocks is shown in *figs. 16* and *17*. The components are assembled on two printed wiring boards, which are connected by sturdy wire interconnections. The boards are then supplied with connection wires (pins) and folded to-

gether. A plastic strip with holes drilled in it keeps the two rows of pins in the right position. The complete unit is then inserted into a metal casing filled with a liquid potting compound. This compound hardens after a short time. A protecting layer of epoxy resin is then applied to prevent moisture from entering, and finally a plastic cover is fitted. The potting compound hardens to a rubbery consistency and prevents shock of vibration from causing relative movement of the components, which could lead to fracture of the connecting wires. Potting also ensures good transfer of heat to the wall of the unit. Since not all of the circuits are of the same size, there are two sizes of casing: the dimensions of a block are either $54.9 \times 14.7 \times 19.5$ mm or $54.9 \times 14.7 \times 27.0$ mm.

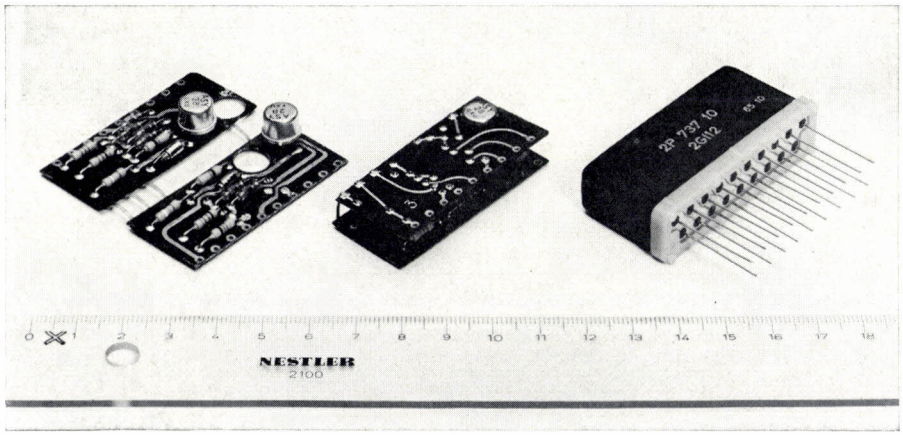

Fig. 16. The interior of the circuit blocks. The circuit is arranged on two printed wiring boards which are folded together and inserted into a metal casing filled with a rubbery compound.

The system also includes a few types of printed circuit board on which the circuit blocks can be arranged, but the user will more often have to design these himself. Care has, however, been taken as far as possible to distribute the various connections among the pins on the units in such a way that these boards need not be excessively complicated. The connections are therefore arranged as follows: the power supply connections are located at one end, with the S and T inputs next to them. These points can therefore be reached by conductors along the edge of the board. Next to the T inputs are the outputs, with the G inputs at the other end. Care has been taken to ensure that points that are most frequently connected will be close together after the circuit block has been placed on the board. These measures usually avoid the crossing of wires on the board, so that single-sided printed wiring boards can be used. These apparently trivial considerations do nevertheless have considerable effect on the design costs of a piece of equipment.

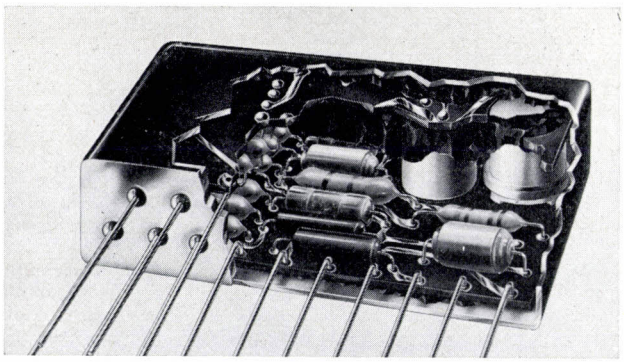

Fig. 17. Sectional view of a circuit block. (In the present design the pins come out through a cap of a different shape.)

Designing circuit blocks

Finally, we shall briefly examine the method used in designing the blocks. The designs must satisfy much more stringent requirements than those for the various circuits in say a radio receiver, if the reject rate in production is to be kept within reasonable bounds.

All the components used to construct a circuit deviate to a certain degree from their nominal values. The largest permissible deviation (tolerance) is determined for each component by several different factors. If it so happens that all the components in a circuit have values close to the tolerance limits and if these faults affect the result in the same sense, the result will be very poor. The likelihood of this in a circuit made up from a large number of components, e.g. a radio set, is very small, and in such a case no special action is required. The situation is quite different however in a digital equipment. A standard signal with a certain tolerance must be supplied to the output of each stage, and each stage must, therefore, be "good". Moreover, in such a stage there are sometimes only four or five components in the circuit, and the likelihood of the coincidence of the most unfavourable values for these components is far from small.

For these reasons, the "worst case" method is often followed in the design of digital circuits [6]. Here, the circuits are designed so that they will still operate properly even if the values of the components are at the least favourable values (but, of course, still within the limits of the tolerance). There will, therefore, be no rejects due to the inevitable spread during manufacture. One of the results of this method is that most circuits are better than calculated, and thus better than they need be, and, in nearly every case, much better. This does give the impression that the worst case method is not the most economical one.

There is another possible method, the "statistical" method, in which a small reject rate is accepted. It can only be used however if a few conditions are satisfied. First, there must be no correlation between the deviations in the various values. This condition is met by the actual values of different components, but when dealing for instance with the current amplification and the cut-off frequency of the same transistor, this condition does not necessarily apply.

Secondly, the nature of the distribution of the deviation must be known. Although a nominal value and two tolerance limits are always given, the distribution can still take many forms within these limits (*fig. 18*). The normal distribution in fig. 18*a* is seldom met with in practice. The distribution in fig. 18*b* is often found, with a peak whose position changes during the production of the component. This arises because the production process is checked and readjusted only when the tolerance limits are exceeded. The distribution in fig. 18*c* is found with values that are difficult to measure. The tolerance limits taken by the manufacturer are then, of necessity, very wide, and inspection is made by sample testing to find out whether the product is still in tolerance. It often happens, too, that the manufacturer divides the product into two or more groups by setting an arbitrary limit. This gives two chopped normal distributions (fig. 18*d*). The position here becomes even more complicated if the peak of the distribution shifts in time or if the manufacturer modifies the selection limit in order to obtain smaller or larger quantities of one of the types.

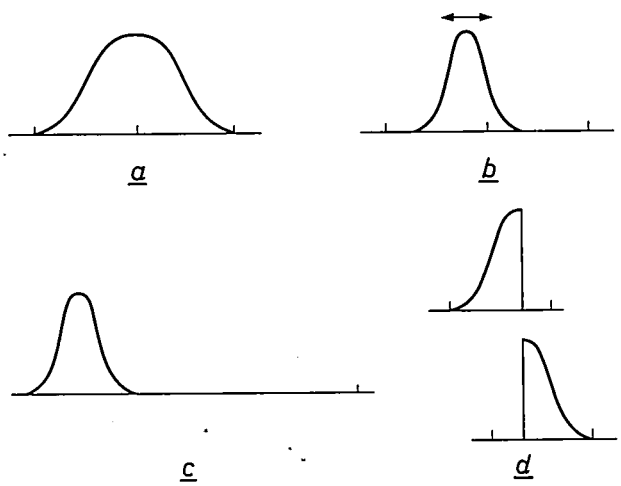

Fig. 18. The different distributions which the value of a component can have within its tolerance limits.

It will be clear that, with such distribution of the components, it is extremely difficult to obtain suitable data for a statistical design. Furthermore, the method is laborious. Of course, the calculations can be made by an electronic computer, but the programming alone requires a great deal more work than ordinary "pencil and paper" calculation of the "worst case" design for the same unit.

The statistical method has been used only to a limited extent for the circuit blocks described in this article. The worst case method has usually been used. In this method, an extra margin of safety has also been included in the calculations to allow for the component ageing determined by life tests. In this approach we have endeavoured to ensure the maximum long-term reliability, something which, particularly in the industrial field, is of vital importance.

[6] A. I. Pressman, Design of transistorized circuits for digital computers, Rider, New York 1959.
W. Roehr and J. Kane, Transistor flip-flops — worst-case design is your best bet, Electronic Design **11**: No. 23, p. 58; No. 24, p. 54; No. 25, p. 60; 1963.
W. D. Ashcraft and W. Hochwald, Design by worst-case analysis: a systematic method to approach specified reliability requirements, IRE Trans. on reliability and quality control **RQC-10**, No. 3, 15-21, 1961.
W. Bongenaar and N. C. de Troye, Worst-case considerations in designing logical circuits, IEEE Trans. on electronic computers **EC-14**, 590-599, 1965.

Summary. Digital equipment is made up of a large number of circuits of only a few basic types. These circuits are manufactured as "ready-made" circuit blocks which can easily be fitted to printed wiring boards. Both the design and assembly of digital equipment have been made much simpler and cheaper with these circuit blocks than they would be with conventional components. The article describes two series of circuit blocks, the 10-series and the 20-series, made by Philips. These series include virtually all the circuits normally found in digital equipment, i.e. not only bistable circuits, trigger gates and logic circuits, but also such less frequently occurring types as clock pulse generators, time-delay units, output amplifiers, etc. The discussion includes the measures taken to combine these circuit blocks as simply as possible to form a complete equipment. To this end, the currents and voltages at the inputs and outputs of the circuit blocks, as well as the signal edges during the transitions from high to low voltage and vice versa, have been standardized to a high degree. The loadability of the circuit blocks can thus be described in very concise loading tables. It follows from the principles chosen for the logic circuits that only NAND circuits are used; this system is explained in detail. Finally, attention is paid to the design of the circuit blocks, based mainly on the "worst case" method.